WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a CPU;

an auxiliary operational device for the CPU, the device composed of a programmable device which can reprogram a circuit configuration thereof;

first diagnosing means for receiving one or more instructions and diagnosing whether the one or more instructions is a reserved instruction that can be processed by the auxiliary operational device or not; and

a configuration controller for programming circuit configuration data for executing processing of the reserved instruction into the auxiliary operational device.

2. The semiconductor integrated circuit according to claim 1, further comprising:

second diagnosing means for diagnosing, upon receipt of a result of the first diagnosing means, whether the circuit for executing processing of the reserved instruction exists in the auxiliary operational device or not in a case where the one or more instructions is the reserved instruction; and

third diagnosing means for diagnosing, upon receipt of diagnosis results of the first diagnosing means and/or the second diagnosing means, whether the processing of the reserved instruction is executed by using the auxiliary operational device or not in a case where the one or more instructions is the reserved instruction.

3. The semiconductor integrated circuit according to

claim 2, further comprising instruction changeover means for instructing, upon receipt of a diagnosis result of the second diagnosing means, to execute the processing of the reserved instruction by the auxiliary operational device in a case where the circuit for executing the processing of the reserved instruction exists in the auxiliary operational device, and for instructing to execute the processing of the reserved instruction by the CPU in a case where no circuit for executing the processing of the reserved instruction exists in the auxiliary operational device.

4. The semiconductor integrated circuit according to claim 3, wherein

the reserved instruction is an instruction that cannot be executed by the CPU,

the semiconductor integrated circuit further comprises substitute instruction supplying means for supplying a substitute instruction in order to execute a substantially equivalent processing to the reserved instruction by the CPU, and

the instruction changeover means has a function for fetching the substitute instruction from the substitute instruction supplying means.

5. The semiconductor integrated circuit according to claim 3, wherein

the reserved instruction is an instruction that cannot be executed by the CPU,

the semiconductor integrated circuit further comprises

instruction supplying means having a function for supplying the one or more instructions and a substitute instruction for executing a substantially equivalent processing to the reserved instruction by the CPU, and

the instruction changeover means has a function for selecting and obtaining the reserved instruction or the substitute instruction from the instruction supplying means.

6. The semiconductor integrated circuit according to claim 3, wherein

the reserved instruction is an instruction that can be executed by the CPU,

the instruction changeover means has a function for changing the instruction so that the processing of the reserved instruction is executed by the auxiliary operational device in a case where the processing of the reserved instruction is executed by the auxiliary operational device, and for not changing the reserved instruction in a case where the processing of the reserved instruction is executed by the CPU.

7. The semiconductor integrated circuit according to claim 1, wherein

the configuration controller has a function for programming, upon receipt of the reserved instruction, circuit configuration data of the reserved instruction into the auxiliary operation device in a case where no circuit for executing the processing of the reserved instruction exists in the auxiliary operation device.

8. The semiconductor integrated circuit according to claim 1, further comprising history storage means for storing usage frequency of the reserved instruction,

wherein the configuration controller programs, while referring to the history storage means, circuit configuration data for processing the reserved instruction with higher usage frequency into the auxiliary operational device with priority.

9. The semiconductor integrated circuit according to claim 8, further comprising a memory,

wherein the configuration controller programs, while referring to the history storage means, the circuit configuration data of the reserved instruction into the auxiliary operational device and the memory in the order of high usage frequency.

10. The semiconductor integrated circuit according to claim 8, further comprising a memory,

wherein the configuration controller further includes fourth diagnosing means for programming, while referring to the history storage means, the circuit configuration data of the reserved instruction into the auxiliary operational device if an idle capacity is larger than the circuit configuration data of the reserved instruction, and for releasing, if the idle capacity is smaller than the data of the reserved instruction, reserved instruction having lower usage frequency than that of the reserved instruction from the auxiliary operational device until the idle capacity

becomes larger than the circuit configuration data of the reserved instruction, and for programming the released reserved instruction into the memory.

11. The semiconductor integrated circuit according to claim 1, further comprising history storage means for storing a transition pattern of the reserved instruction when the one or more instructions includes a plurality of reserved instructions,

wherein the configuration controller programs, while referring to the history storage means, the circuit configuration data of the reserved instruction having a higher probability of transition from a reserved instruction being received at present into the auxiliary operational device with priority.

12. The semiconductor integrated circuit according to claim 1, further comprising history storage means for storing for each reserved instruction a frequency of a second reserved instruction executed next to a first reserved instruction when the one or more instructions includes a plurality of reserved instructions are received,

wherein the configuration controller programs, while referring to the history storage means, the circuit configuration data of the second reserved instruction having a high frequency of being executed next to the first reserved instruction being received at present into the auxiliary operational device with priority.

13. The semiconductor integrated circuit according to

claim 1, further comprising history storage means for storing a transition pattern of the reserved instruction in a case where the reserved instruction is received two times, and a time interval at which the two reserved instructions are received,

wherein the configuration controller programs, while referring to the history storage means, the circuit configuration data of the reserved instruction having a higher transition probability from a reserved instruction being received at present into the auxiliary operational device only when the time interval is longer than a time required for programming the circuit configuration data.

14. The semiconductor integrated circuit according to claim 1, further comprising history storage means for storing a transition pattern of the reserved instruction in a case where the reserved instruction is received two times, and a time interval at which the two reserved instructions are received,

wherein the configuration controller programs, while referring to the history storage means, the circuit configuration data of a second reserved instruction having a high frequency of being executed next to a first reserved instruction being currently received into the auxiliary operational device only when the time interval is longer than a time required for programming the circuit configuration data.

15. The semiconductor integrated circuit according to

claim 1, wherein

the configuration controller programs the configuration data of the reserved instruction if an idle capacity of the auxiliary operational device is larger than a capacity of the configuration data of the reserved instruction, and releases, if the idle capacity is smaller than a capacity of the configuration data of the reserved instruction, a reserved instruction having lower usage frequency than the reserved instruction from the auxiliary operational device until the idle capacity becomes larger than the capacity of circuit configuration data of the reserved instruction.

16. The semiconductor integrated circuit according to claim 1, wherein

the auxiliary operational device has a plurality of banks, and

the configuration controller programs the configuration data of the reserved instruction if a vacant bank of the auxiliary operational device is larger than a necessary bank of the configuration data of the reserved instruction, and releases, if the vacant bank is smaller than a necessary bank of the configuration data of the reserved instruction, a reserved instruction having a lower usage frequency than the reserved instruction from the auxiliary operational device until the vacant bank becomes larger than the necessary bank of the circuit configuration data of the reserved instruction.